**Remarks/Arguments**

The Examiner is thanked for the thorough examination and search of the subject patent application.

Claims 15, 27, 35-39 and 41 are pending; Claims 15, 27 and 37 have been currently amended; Claims 1-14, 16-26, 28-34 and 40 have been canceled. No new matter is believed to have been added.

Response to Claim Rejections under 35 U.S.C. 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

**Response to Claims 15 and 35**

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As currently amended, independent Claim 15 is recited, as below:

15. A method for fabricating a circuit component, comprising:

providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening;

providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, and wherein said exposed metallization structure comprises a metal bump used for a package interconnect, wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump; and

after said providing said exposed metallization structure, performing a sputter etching process with an argon gas.

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*Reconsiderations of Claim 15 rejected under 35 U.S.C. 102(e) as being anticipated by Kajiwara et al. (U.S. Pub. No. 2003/0127747), of Claim 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara et al. in view of Hikita et al. (U.S. Pub. No. 2003/0146518) and of Claim 35 rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara et al. in view of Dass et al. (U.S. Pat. No. 6,162,652) are requested in accordance with the following remarks.*

Claim 15 has been currently amended as the subject matter previously claimed in Claim 17 has been currently added into Claim 15 and is believed to patentably distinguish over the citations by Kajiwara et al. (U.S. Pub. No. 2003/0127747) in view of Hikita et al. (U.S. Pub. No. 2003/0146518).

The Examiner considers that "because both references teach methods of forming metal bumps for external electrical connection in a semiconductor device, it would have been obvious to one skilled in the art to substitute one method for the other to achieve the predictable results of having the suitable bump design for the required device manufacturing process." ~ *See lines 2-6 on page 4, in the last Office Action mailed Feb. 18, 2009* ~

Applicants respectfully traverse the Examiner's opinion. Kajiwara et al. teach that an Au bump 7 on an Al electrode pad is formed by a ball bonding method using supersonic hot press bonding and a surface of the Au bump 7 is sputter etched by an Ar gas. ~ *See Fig. 1 and col. 5, lines 1-3 and 12-17, in U.S. Pub. No. 2003/0127747* ~ Hikita et al. teach that a metal bump 3,

such as Au, Pd, Pt, Ag and Ir, is formed using an electroplating process or an electroless plating process. ~ *See Fig. 3 and para. [0051], in U.S. Pub. No. 2003/0146518* ~ However, both Kajiwara et al. and Hikita et al. fail to teach, hint or suggest that an electroplated or electroless plated metal bump need to be sputter etched. It is believed to be unobvious to apply Hikita et al.'s metal bump 3 to Kajiwara et al.'s Au bump 7 because both Kajiwara et al. and Hikita et al. fail to teach, hint or suggest that an electroplated or electroless plated metal bump, such as Hikita et al.'s metal bump 3, need to be sputter etched.

For at least the foregoing reasons, withdrawal of the rejection to Claim 15 under 35 U.S.C. 102(e) is respectfully requested.

Applicants respectfully submit independent Claim 15 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claim 35 patentably define over the prior art as well.

**Response to Claims 27 and 36**

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As currently amended, independent Claim 27 is recited below:

27. A method for fabricating a circuit component, comprising:

providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer over said semiconductor wafer and on said second region, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening;

providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, and wherein said exposed metallization structure comprises a metal bump used for a package interconnect, wherein said metal bump has

a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump; and

after said providing said exposed metallization structure, performing an ion milling process with an argon gas.

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*Reconsiderations of Claim 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara et al. (U.S. Pub. No. 2003/0127747) in view of Fan et al. (U.S. Pat. No. 6,956,292), of Claim 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara et al. in view of Fan et al., further in view of Hikita et al. (U.S. Pub. No. 2003/0146518) and of Claim 36 rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara et al. in view of Fan et al., further in view of Dass et al. (U.S. Pat. No. 6,162,652) are requested in accordance with the following remarks.*

Claim 27 has been currently amended as the subject matter previously claimed in Claim 30 has been currently added into Claim 27 and is believed to patentably distinguish over the citations by Kajiwara et al. (U.S. Pub. No. 2003/0127747) in view of Fan et al. (U.S. Pat. No. 6,956,292), further in view of Hikita et al. (U.S. Pub. No. 2003/0146518).

The Examiner considers that "because both references teach methods of forming metal bumps for external electrical connection in a semiconductor device, it would have been obvious to one skilled in the art to substitute one method for the other to achieve the predictable results of having the suitable bump design for the required device manufacturing process." *~ See lines 2-6 on page 4, in the last Office Action mailed Feb. 18, 2009 ~*

Applicants respectfully traverse the Examiner's opinion. Kajiwara et al. teach that an Au bump 7 on an Al electrode pad is formed by a ball bonding method using supersonic hot press bonding and a surface of the Au bump 7 is sputter etched by an Ar gas. ~ *See Fig. 1 and col. 5, lines 1-3 and 12-17, in U.S. Pub. No. 2003/0127747* ~ Hikita et al. teach that a metal bump 3, such as Au, Pd, Pt, Ag and Ir, is formed using an electroplating process or an electroless plating process. ~ *See Fig. 3 and para. [0051], in U.S. Pub. No. 2003/0146518* ~ However, both Kajiwara et al. and Hikita et al. fail to teach, hint or suggest that an electroplated or electroless plated metal bump need to be sputter etched. It is believed to be unobvious to apply Hikita et al.'s metal bump 3 to Kajiwara et al.'s Au bump 7 because both Kajiwara et al. and Hikita et al. fail to teach, hint or suggest that an electroplated or electroless plated metal bump, such as Hikita et al.'s metal bump 3, need to be sputter etched.

For at least the foregoing reasons, withdrawal of the rejection to Claim 27 under 35 U.S.C. 103(a) is respectfully requested.

Applicants respectfully submit independent Claim 27 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claim 36 patentably define over the prior art as well.

**Response to Claims 37-39 and 41**

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As currently amended, independent Claim 37 is recited below:

37. A method for fabricating a circuit component, comprising:

providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening;

providing an exposed metallization structure directly on said passivation layer, on said first region and over said semiconductor wafer, wherein said exposed metallization structure is connected to said first region through said opening, and wherein said exposed metallization structure comprises a metal bump used for a package interconnect, wherein said metal bump has a substantially vertical sidewall extending from a bottom of said metal bump to a substantially planar top surface of said metal bump; and

after said providing said exposed metallization structure, performing an ion milling process with an inert gas.

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*Reconsiderations of Claims 37 and 38 rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara et al. (U.S. Pub. No. 2003/0127747) in view of Fan et al. (U.S. Pat. No. 6,956,292), of Claim 39 rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara et al. in view of Fan et al., further in view of Zhang et al. (U.S. Pat. No. 6,104,461), of Claim 40 rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara et al. in view of Fan et al., further in view of Hikita et al. (U.S. Pub. No. 2003/0146518) and of Claim 41 rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara et al. in view of Fan et al., further in view of Dass et al. (U.S. Pat. No. 6,162,652) are requested in accordance with the following remarks.*

Claim 37 has been currently amended as the subject matter previously claimed in Claim 40 has been currently added into Claim 37 and is believed to patentably distinguish over the citations by Kajiwara et al. (U.S. Pub. No. 2003/0127747) in view of Fan et al. (U.S. Pat. No. 6,956,292), further in view of Hikita et al. (U.S. Pub. No. 2003/0146518).

The Examiner considers that "because both references teach methods of forming metal bumps for external electrical connection in a semiconductor device, it would have been obvious to one skilled in the art to substitute one method for the other to achieve the predictable results of having the suitable bump design for the required device manufacturing process." *~ See lines 2-6 on page 4, in the last Office Action mailed Feb. 18, 2009 ~*

Applicants respectfully traverse the Examiner's opinion. Kajiwara et al. teach that an Au bump 7 on an Al electrode pad is formed by a ball bonding method using supersonic hot press bonding and a surface of the Au bump 7 is sputter etched by an Ar gas. *~ See Fig. 1 and col. 5, lines 1-3 and 12-17, in U.S. Pub. No. 2003/0127747 ~* Hikita et al. teach that a metal bump 3, such as Au, Pd, Pt, Ag and Ir, is formed using an electroplating process or an electroless plating process. *~ See Fig. 3 and para. [0051], in U.S. Pub. No. 2003/0146518 ~* However, both Kajiwara et al. and Hikita et al. fail to teach, hint or suggest that an electroplated or electroless plated metal bump need to be sputter etched. It is believed to be unobvious to apply Hikita et al.'s metal bump 3 to Kajiwara et al.'s Au bump 7 because both Kajiwara et al. and Hikita et al. fail to teach, hint or suggest that an electroplated or electroless plated metal bump, such as Hikita et al.'s metal bump 3, need to be sputter etched.

For at least the foregoing reasons, withdrawal of the rejection to Claim 37 under 35 U.S.C. 103(a) is respectfully requested.

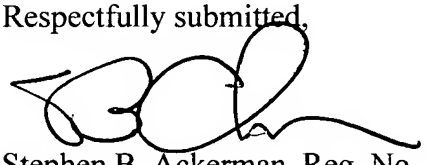
Applicants respectfully submit independent Claim 37 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 38, 39 and 41 patentably define over the prior art as well.

Conclusion

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should the Examiner not find that the Claims are now Allowable that the Examiner call the undersigned at 845-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,



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